ABSTRACT OF THE DISCLOSURE

A non-volatile memory array structure, comprising a plurality of first transistors, serving for memory function, being arranged to have a plurality of columns and a plurality of first rows. The first transistors in each column are coupled in series, and adjacent two of the columns are grouped into a memory group using a common bit line. The gate electrodes of the first transistors in the same first row are coupled with a first sequence word line. A plurality of second transistors are also included. Each of the second transistors is coupled between two columns of the memory group and is adjacent to each of the first rows. The second transistors form a plurality of second rows, wherein gate electrodes of the second transistors in the same second row are coupled to a second sequence word line.